In the Claims:

1. (Currently Amended) A method for manufacturing a trench structure having sidewalls a lower portion and an upper portion ~~formed in a depth under the surface of a semiconductor substrate~~, said method comprising:

providing ~~said~~ a semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching;

defining at the surface of the semiconductor substrate first areas of a rectangular surface grid having an x axis and a y axis, said x and y axes of the surface grid positioned to be parallel to the crystal faces that are less resistant to etching;

etching a surface opening of said trench structures in said first areas, wherein the upper portion of the trench structure comprises sidewalls substantially parallel to the crystal faces that are less resistant to etching; and

etching said lower portion ~~sidewalls~~ of the trench structures in order to form sidewalls which are substantially parallel to the crystal faces that are more resistant to etching ~~formed in a depth under said surface of said semiconductor substrate by etching said crystal faces that are less resistant to etching so as to expand said sidewalls beneath said first areas of said surface grid~~.

2. (Previously Presented) The method of claim 21, wherein said surface opening of a trench structure opening is imaged onto the first areas of the surface of the semiconductor substrate by means of an exposure device.

3. (Previously Presented) The method of claim 2, wherein prior to imaging, a mask opening defining rectangular sides in a layout of the trench structure is oriented so that the rectangular sides are parallel with the crystal faces of the semiconductor substrate that are less resistant to etching.

4. (Previously Presented) The method of claim 21, wherein the semiconductor substrate comprises a semiconductor wafer that includes a marking identifying a crystal orientation of the crystal lattice.

5. (Previously Presented) The method of claim 4, wherein the marking identifies the orientation of the crystal faces that are less resistant to etching.

6. (Original) The method of claim 5, wherein the marking is used for the orientation of a mask in an exposure device.

7. (Previously Presented) The method of claim 21, further comprising etching an opening at the surface of the semiconductor substrate with an oval cross section.

8. (Previously Presented) The method of claim 21, wherein the semiconductor substrate comprises monocrystalline silicon.

9. (Original) The method of claim 8, wherein the surface grid is oriented in accordance with a <100> crystal orientation of the monocrystalline silicon.

10. (Previously Presented) The method of claim 9, wherein the <100> crystal faces comprise the crystal faces that are less resistant to etching and the <110> crystal faces comprise the crystal faces that are more resistant to etching.

11. (Previously Presented) The method of claim 21, further comprising providing upper sections of the trench structures, between the surface of the semiconductor substrate and at least one lower edge of the secondary structures, with a protective layer that is resistant to the etching process that expands said sidewalls of said trench structure.

12. (Previously Presented) The method of claim 21, wherein the trench structures are functionally designed as storage capacitances.

13. (Previously Presented) The method of claim 12, wherein the secondary structures comprise selection transistors formed in the second areas for use with the storage capacitances of DRAM cells.

14-20. (Canceled)

21. (Currently Amended) A method for increasing a structure size of trench structures in a depth under a surface of a semiconductor substrate, said method comprising:

providing said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching;

defining first areas for forming said trench structures ~~in a checker-board fashion~~ in a rectangular surface grid having an x axis and a y axis [[,]] at a surface of the semiconductor

substrate[[,]];

defining second areas ~~said first areas alternating with second areas~~ for forming secondary structures in a section of the semiconductor substrate that is near a surface thereof, said second areas alternating with first areas, said x axis and y axis of the surface grid positioned to be parallel to the crystal faces that are less resistant to etching; and

performing area-selective etching to increase the structure size of the trench structures in said depth under said semiconductor substrate's surface, said structure size of said trench structures expanded along said crystal faces that are less resistant to etching beneath said second areas for forming said secondary structures by said area selective etching.

22. (Currently Amended) The method of claim 1, wherein a rectangular opening of a mask ~~trench structure~~ is imaged onto the surface of the semiconductor substrate forming a trench structure, ~~by means of an exposure device~~ wherein the trench structure is aligned with the x, and y axes of the surface grid ~~parallel to the crystal faces of the semiconductor substrate that are less resistant to etching~~.

23. (Currently Amended) The method of claim 22, wherein the rectangular opening ~~prior to said imaging, a~~ of the mask having ~~rectangular mask openings in a layout of the large structure~~ a long side and a short side and wherein ~~is oriented such that~~ the sides of the rectangular mask opening are oriented parallel ~~with~~ to the crystal faces of the semiconductor substrate that are less resistant to etching.

24. (Previously Presented) The method of claim 1, wherein the semiconductor substrate comprises a semiconductor wafer that includes a marking identifying a crystal orientation of the crystal lattice.

25. (Previously Presented) The method of claim 24, wherein the marking identifies the orientation of the crystal faces that are less resistant to etching.

26. (Previously Presented) The method of claim 25, wherein said marking is used for orienting a patterned mask.

27. (Previously Presented) The method of claim 1, wherein etching a surface opening of the trench comprises etching with an oval cross section.

28. (Currently Amended) A method for manufacturing a trench structure having ~~sidewalls formed in a depth under the surface of a semiconductor substrate~~ a lower portion and an upper portion, said method comprising:

providing said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching;

defining at the surface of the semiconductor substrate ~~first areas of~~ a ~~rectangular~~ checker-board surface grid having an x axis and a y axis, ~~said~~ first areas being located in the checker-board surface grid ~~fashion for forming said trench structures~~, said first areas alternating with second areas of said ~~rectangular~~ checker-board surface grid, said first areas being provided for forming said trench structures, said second areas being provided for forming secondary structures

in a section of the semiconductor substrate that is near said surface thereof, said x and y axes of the checker-board surface grid positioned to be parallel to the crystal faces that are less resistant to etching; ~~and~~

~~etching a surface opening of said trench structures in said first areas~~

forming sidewalls of the upper portion of the trench structure in said first areas wherein the sidewalls are substantially parallel to the crystal faces that are less resistant to etching; and

forming sidewalls of the lower portion of the trench structure wherein the sidewalls of the lower portion are substantially parallel to crystal faces that are more resistant to etching.

29. (Previously Presented) The method of claim 28, wherein the secondary structures comprise selection transistors.

30. (Currently Amended) The method of claim 28, wherein a rectangular opening of a mask ~~trench structure~~ is imaged onto the surface of the semiconductor substrate forming a trench structure, ~~by means of an exposure device~~ wherein the trench structure is aligned with the x, and y axes of the checker-board surface grid ~~parallel to the crystal faces of the semiconductor substrate that are less resistant to etching~~.

31. (Currently Amended) The method of claim 30, wherein the rectangular opening ~~prior to said imaging, a~~ of the mask ~~having rectangular mask openings in a layout~~ is oriented such that the sides of the rectangular ~~mask~~ opening of the mask are parallel ~~with~~ to the crystal faces of the semiconductor substrate that are less resistant to etching.

32. (Previously Presented) The method of claim 28, wherein the semiconductor substrate comprises a semiconductor wafer having a marking identifying a crystal orientation of the crystal lattice.

33. (Previously Presented) The method of claim 32, wherein the marking identifies the orientation of the crystal faces that are less resistant to etching.

34. (Previously Presented) The method of claim 33, further comprising using said marking for orienting a patterned mask.

35. (Previously Presented) The method of claim 28, wherein etching the surface opening comprises etching with an oval cross section.

36. (Currently Amended) A method of fabricating a semiconductor device, the method comprising:

providing a silicon substrate having <100> crystal faces and <110> crystal faces;

forming an array of rows and columns of trench structures at a surface of the semiconductor substrate, the rows and columns being parallel to the <100> crystal faces, the etching comprising:

etching the semiconductor substrate to form upper portions of the trench structures, the upper portions of the trench structures having side walls substantially parallel to the <100> crystal faces;

forming a protective layer over the upper portions of the trench structures; and

etching the semiconductor substrate to form lower portions of the trench structures

beneath the upper portions, the lower portions being wider than the upper portions and comprise a substantially rectangular shape with side walls substantially parallel to the <110> crystal faces.

37. (Currently Amended) The method of claim 36, wherein etching the semiconductor substrate to form upper portions of the trench structures comprises forming upper portions that each have a substantially oval shape ~~with long sides oriented parallel to the <100> crystal face~~.

38. (Canceled)

39. (Previously Presented) The method of claim 36, further comprising forming a plurality of capacitor, each capacitor being formed in an associated one of the trench structures.

40. (Previously Presented) The method of claim 39, further comprising a plurality of secondary structures, each secondary structure comprising an access transistor functionally coupled to one of the capacitors.

41. (Currently Amended) The method of claim 40, wherein the lower portions of the ~~trenches~~ trench structures extend beneath the access transistor of the secondary structures.

42. (Previously Presented) The method of claim 36, wherein the semiconductor substrate comprises a semiconductor wafer having a marking identifying a crystal orientation of the crystal lattice.

43. (Previously Presented) The method of claim 42, wherein the marking identifies the crystal orientation of the <100> crystal faces.

44. (Currently Amended) The method of claim 43, further comprising forming a patterned mask aligned with the marking before ~~wherein~~ etching the semiconductor substrate to form upper portions of the trench structures ~~comprises using the marking to orient a patterned mask~~.